## Chenghao Feng


CONTACT INFORMATION

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RESEARCH INTERESTS

Silicon photonics, design, simulation, and testing of photonic integrated circuits (PIC) for digital computing and interconnect, photonic neuromorphic computing

EDUCATION

**The University of Texas at Austin**, Austin, TX

Ph.D. student, Department of Electrical and Computer Engineering (Aug. 2018-Present)

- Advisor: Ray T. Chen
- Co-advisor: David Z. Pan

**Nanjing University**, Nanjing, China

B.S. in Physics, (2014-2018)

WORK EXPERIENCE

**Meta Platforms**, Menlo park, CA, USA. **May, 2022 - Aug, 2022**

*Hardware engineer intern, Meta NWE Network Team, Optical Technologies group*

- **2x400G optics validation:** Worked on host compliance test for 2x400G OSFP optical modules; Worked on unifying HTX settngs of 2x400G optical modules .
- **Silicon photonic device design:** Built a fully-automated design flow to run FDTD/MODE simulations on Lumerical using Python APIs. Designed photonic devices using foundry process files.

RESEARCH PROJECTS

**The University of Texas at Austin**, Austin, TX, USA. **August, 2018 - present**

*Graduate research assistant*

- **Hardware-efficient photonic neural chip:** Worked on photonic neural chip tape-out for novel optical neural network(ONN) architectures using Advanced Micro Foundry (AMF); worked on the full-stack schematic design, layout, validation of photonic neural chips using Lumerical Device/Mode/Interconnect, Synopsys optodesigner, and PyTorch; worked on optoelectronic co-packaging and controlling circuit design; built the programmable testing setup using Python APIs; tested the performance of the photonic neural chip. Proposed and demonstrated a hardware-efficient photonic neural network architecture.
- **Photonic neural network hardware-software co-design:** Collaborated on designing high-throughput and low-power photonic ONN architectures ; helped verify the functionality of photonic parts using Lumerical Interconnect.
- **Electronic-photonic digital computing chip:** Worked on electronic-photonic digital computing chip tape-out for photonic logic functional units using AIM photonics; worked on the design, layout, validation, tape-out, performance evaluation, and high-speed measurement of the digital computing circuits. Proposed and demonstrated an electronic-photonic comparator and an electronic-photonic decoder/multiplexer that can outperform the state-of-the-art transistor-based circuits in speed and power consumption.
- **Electronic-photonic digital full adder:** Collaborated on the architecture design, high-speed measurement, and performance evaluation of an electronic-photonic full adder fabricated by AIM photonics. Collaborated on proposing and the idea of electronic-photonic arithmetic logic unit.

- **Modeling of high-speed silicon photonic modulators:** Modeled and analyzed high speed properties of cascaded EO microring/microdisk modulators in optical computing systems using Matlab and Lumerical Interconnect. Provided the solutions to increase the optical bandwidth of the microresonator-based modulators and the accuracy of the optical digital computing circuits.

**Nanjing University**, Nanjing, China. **August, 2017 - June, 2018**

*Undergraduate research student*

- **Arbitrary Complex Brag Grating Waveguide:** Developed and optimized codes to design the arbitrary complex Brag grating waveguide using inverse-design algorithms. Improved the simulation time complexity and scaled down the size of the structure using MATLAB, Lumerical MODE, and Lumerical FDTD. Modeled the dispersion of silicon Brag grating waveguide and improved the simulation accuracy.
- **The Electrical Properties of a P-I-N-based optical Modulator :** Analyzed the impedance and modulation performance of a p-i-n-diode-based electrooptical modulator under high modulation frequency using Lumerical DEVICE and MODE.

## Journal Publications

1. Jiaqi Gu, **Chenghao Feng**, Hanqing Zhu, Zheng Zhao, Zhoufeng Ying, Mingjie Liu, Ray T. Chen, and David Z. Pan, "SqueezeLight: A Multi-Operand Ring-Based Optical Neural Network with Cross-Layer Scalability," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Jul. 2022
2. Hanqing Zhu, Jiaqi Gu, **Chenghao Feng**, Mingjie Liu, Zixuan Jiang, Ray T. Chen, and David Z. Pan, "ELight: Towards Efficient and Aging-Resilient Photonic In-Memory Neurocomputing," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Jun. 2022
3. Jiaqi Gu, **Chenghao Feng**, Hanqing Zhu, Ray T. Chen, and David Z. Pan, "Light in AI: Toward Efficient Neurocomputing with Optical Neural Networks - A Tutorial," IEEE Transactions on Circuits and Systems–II: Express Briefs (TCAS-II), Apr. 2022.
4. **Chenghao Feng**, Zhoufeng Ying, Zheng Zhao, Jiaqi Gu, David Z. Pan, and Ray T. Chen, "Toward high-speed and energy-efficient computing: A WDM-based scalable on-chip silicon integrated optical comparator", Laser and Photonics Reviews 2021, 15, 2000275
5. Zhoufeng Ying, **Chenghao Feng**, Zheng Zhao, et al. "Sequential logic and pipelining in chip-based electronic-photonic digital computing", IEEE Photonics Journal, 2020, 12(6): 1-11.
6. **Chenghao Feng**, Zhoufeng Ying, Zheng Zhao, Jiaqi Gu, David Z. Pan, and Ray T. Chen. "Wavelength-division-multiplexing (WDM)-based integrated electronic–photonic switching network (EPSN) for high-speed data processing and transportation", Nanophotonics, vol. 9, no. 15, 2020, pp. 4579-4588.
7. Jiaqi Gu, Zheng Zhao, **Chenghao Feng**, Zhoufeng Ying, Mingjie Liu, Ray T Chen, David Z Pan. "Towards Hardware-Efficient Optical Neural Networks: Beyond FFT Architecture via Joint Learnability", IEEE Transaction on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Sept., 2020.
8. Zhoufeng Ying, **Chenghao Feng**, Zheng Zhao, et al. "Electronic-photonic arithmetic logic unit for high-speed computing", Nature communications, 2020, 11(1): 1-9.
9. **Chenghao Feng**, Zhoufeng Ying, Zheng Zhao, Rohan Mital, David Z. Pan and Ray T. Chen. "Analysis of microresonator-based logic gate for high-speed optical computing in integrated photonics", IEEE Journal of Selected Topics in Quantum Electronics, 2019, 26(2): 1-8.
10. Zhoufeng Ying, **Chenghao Feng**, Zheng Zhao, et al. "Integrated multi-operand electro-optic logic gates for optical computing", Applied Physics Letters, 2019, 115(17): 171104.

11. Zhoufeng Ying, Zheng Zhao, **Chenghao Feng**, Rohan Mital, Shounak Dhar, David Z Pan, Richard Soref, Ray T Chen. "Automated logic synthesis for electro-optic logic-based integrated optical computing", Optics express 26 (21), 28002-28012, 2019.
12. Zhoufeng Ying, Shounak Dhar, Zheng Zhao, **Chenghao Feng**, Rohan Mital, Chi-Jui Chung, David Z Pan, Richard A Soref, Ray T Chen, "Electro-optic ripple-carry adder in integrated silicon photonics for optical computing", IEEE Journal of Selected Topics in Quantum Electronics 24 (6), 1-10.
13. **Chenghao Feng**, Richard Soref, Ray T. Chen, et al. Efficient and accurate synthesis of complex Bragg grating waveguide in dispersive silicon structures[J]. JOSA B, 2018, 35(8): 1921-1927.

Conference papers

1. **Chenghao Feng**, Jiaqi Gu, Hanqing Zhu, Zhoufeng Ying, Zheng Zhao, David Z. Pan, and Ray T. Chen, "Optoelectronically Interconnected Hardware-Efficient Deep Learning using Silicon Photonic Chips," SPIE Photonics West, Mar. 2022.
2. **Chenghao Feng**, Jiaqi Gu, Hanqing Zhu, David Z. Pan, and Ray T. Chen, "Design and Experimental Demonstration of A Hardware-Efficient Integrated Optical Neural Network," SPIE Photonics West, Mar. 2022
3. Jiaqi Gu, Hanqing Zhu, **Chenghao Feng**, Zixuan Jiang, Mingjie Liu, Shuhan Zhang, Ray T. Chen, and David Z. Pan, "ADEPT: Automatic Differentiable DEsign of Photonic Tensor Cores," ACM/IEEE Design Automation Conference (DAC), Jul. 2022. (Best-in-Track Paper)
4. Hanqing Zhu, Jiaqi Gu, **Chenghao Feng**, et al. "ELight: Enabling Efficient Photonic In-Memory Neurocomputing with Life Enhancement", 2022 27th Asia and South Pacific Design Automation Conference (ASP-DAC). IEEE, 2022: 332-338.
5. Jiaqi Gu, Hanqing Zhu, **Chenghao Feng**, et al. " L2ight: Enabling On-Chip Learning for Optical Neural Networks via Efficient in-situ Subspace Optimization", Conference on Neural Information Processing Systems (NeurIPS), Dec. 7-10, 2021.
6. Jiaqi Gu, Hanqing Zhu, **Chenghao Feng**, et al. " Towards Memory-Efficient Neural Networks via Multi-Level in situ Generation", in International Conference on Computer Vision (ICCV), Oct. 10-17, 2021.
7. **Chenghao Feng**, Jiaqi Gu, Hanqing Zhu, et al. "Experimental Demonstration of a WDM-based Integrated Optical Decoder for Compact Optical Computing," in Conference on Lasers and Electro-Optics, Optical Society of America, 2021, SW3C.3.
8. Jiaqi Gu, **Chenghao Feng**, Zheng Zhao, et al. " Efficient On-Chip Learning for Optical Neural Networks Through Power-Aware Sparse Zeroth-Order Optimization", in Association for the Advancement of Artificial Intelligence (AAAI), Virtual Conference, Feb. 02-09, 2021.
9. **Chenghao Feng**, Jiaqi Gu, Zhoufeng Ying, et al. "Scalable fast-Fourier-transform-based (FFT-based) integrated optical neural network for compact and energy-efficient deep learning", Proc. SPIE 11690, Smart Photonic and Optoelectronic Integrated Circuits XXIII, 116900I (March 2021)
10. **Chenghao Feng**, Zhoufeng Ying, Zheng Zhao,et al. "Wavelength-division-multiplexing-based electronic-photonic integrated circuits for high-performance data processing and transportation", Proc. SPIE 11690, Smart Photonic and Optoelectronic Integrated Circuits XXIII, 116900R (March 2021)
11. Jiaqi Gu, **Chenghao Feng**, Zheng Zhao, Zhoufeng Ying, Ray T Chen, David Z Pan. "Efficient On-Chip Learning for Optical Neural Networks Through Power-Aware Sparse Zeroth-Order Optimization", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), Nov. 02-05, 2020.
12. Jiaqi Gu, Zheng Zhao, **Chenghao Feng**, Wuxi Li, Ray T. Chen and David Z. Pan, "FLOPS: Efficient On-Chip Learning for Optical Neural Networks Through Stochastic Zeroth-Order Optimization", ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jul. 19-23, 2020.

13. **Chenghao Feng**, Zheng Zhao, Zhoufeng Ying, et al. "Compact design of on-chip elman optical recurrent neural network",CLEO: Applications and Technology. Optical Society of America, 2020: JTh2B. 8.
14. **Chenghao Feng**, Zhoufeng Ying, Zheng Zhao, et al. "Integrated WDM-based optical comparator for high-speed computing", 2020 Conference on Lasers and Electro-Optics (CLEO). IEEE, 2020: 1-2.
15. Jiaqi Gu, Zheng Zhao, **Chenghao Feng**, Ray T. Chen and David Z. Pan, "ROQ: A Noise-Aware Quantization Scheme Towards Robust Optical Neural Networks with Low-bit Controls", IEEE Design, Automation Test in Europe Conference Exhibition (DATE), Grenoble, France, Mar. 09-13, 2020.
16. **Chenghao Feng**, Zhoufeng Ying, Zheng Zhao, et al. "Wavelength-division-multiplexing-based electronic-photonic network for high-speed computing", Proc. SPIE 11284, Smart Photonic and Optoelectronic Integrated Circuits XXII, 112840H (9 March 2020)
17. Jiaqi Gu, Zheng Zhao, **Chenghao Feng**, Mingjie Liu, Ray T. Chen and David Z. Pan, "Towards Area-Efficient Optical Neural Networks: An FFT-based Architecture", ACM/IEEE Asian and South Pacific Design Automation Conference (ASP-DAC), Beijing, China, Jan. 13-16, 2020.
18. **Chenghao Feng**, Zhoufeng Ying, Zheng Zhao, et al. "Power and accuracy co-optimization of an optical full adder via optimization algorithms",2019 IEEE Photonics Conference (IPC). IEEE, 2019: 1-2.
19. Zhoufeng Ying, **Chenghao Feng**, Zheng Zhao, David Z Pan, Ray T Chen, "Fully integrated 20 Gbit/s silicon optical computing chip for 4-bit full adders", 2019 IEEE Photonics Conference (IPC), 1-2.

## Honors and Awards

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| Provost's International Graduate Excellence Fellowship. UT Austin | 2018 - 2021 |
| Best paper award. ASP-DAC | 2020 |
| Zheng Gang Scholarship. Nanjing University | 2017 |
| Dalian Institute of Chemical Physics, Chinese Academy of Sciences' Scholarship. | 2016 |
| Top-notch Program Scholarship. Nanjing University | 2015 - 2017 |

## Related Courses

EE 383V-1 Nanophotonics; EE 383P-8 Optical Communications; EE 396K-21 Nanoscale Device Physics/Technology; EE 382M-7 VLSI I; EE 382N-14 High-speed computing arithmetic I; EE 380L-10 Data mining; EE 383V Modern Optics; EE 382N-1 Computer Architecture; ME 397 Intelligent nano-world; EE 381V Unconventional computation; EE-382M Analog integrated circuit design.

## Skills

- **Programming Languages**: Python (PyVISA, lumapi, PyTorch), C, Matlab, Verilog
- **Simulation Tools**: Lumerical Solutions
- **EDA Tools**: Synopsys photonic solutons(Optodesigner, Optsim), Klayout, Cadence Virtuoso(OCEAN), Synopsys Design Compiler
- **Experimental skills**: Die-level and transceiver-level test automaton skills; Familiar with using lab equipment such as DCA, VNA, BERT, tunable laser, OSA and etc; PCB assembly skills; Basic skills of fabrication such as E-beam lithography and plasma-etching.
- **Photonic chip tape-out**: 4+ tape-out experience of large-scale silicon photonic integrated circuits, familiar with 3+ photonic foundries. 4+ years' experience in design, simulation, and modeling of photonic integrated circuits and devices. Basic skills of fabrication such as E-beam lithography and plasma-etching. Experience in PCB design for controlling photonic circuits.
- **Photonic integrated circuit and device design**: Device-level design automation skills using Lumerical Solutions and Python APIs; Familiar with high-speed ring/disk modulators, MZI modulators, filter, phase shifter, thermo-optic switch, and various passive components.