

# JIAQI GU

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## EDUCATION

<b>The University of Texas at Austin</b>	PhD of Electrical and Computer Engineering Architecture, Computer System and Embedded System Track	May 2023
<b>Fudan University, Shanghai, China</b>	Bachelor of Microelectronic Science and Engineering (Eminent Engineer Program) Overall GPA: 3.91/4.00	Jul 2018

## EXPERIENCE

<b>Graduate Research Assistant, The University of Texas at Austin</b>	Jun 2019 – Present
<ul style="list-style-type: none"><li>• Optical neural network architecture design</li><li>• ASIC Placement acceleration with GPUs</li></ul>	
<b>Graduate Research Assistant, The University of Texas at Austin</b>	Sep 2018 – Jan 2019
<ul style="list-style-type: none"><li>• Projected RISC-V Rocket Core on Zynq FPGA and achieved communication between them</li><li>• Customized FIRRTL transformation and built infrastructure for fault injection and system state snapshot</li></ul>	
<b>Research Assistant, Fudan University, Shanghai, China</b>	Aug 2017 – Jul 2018
<ul style="list-style-type: none"><li>• Modified infant brain atlas offered by UNC and created complete tissue probability maps</li><li>• Developed two-stage reconstruction framework for infant thin-section MR image reconstruction by using GANs and CNN; research is developing brand new method to improve reconstruction performance by fusing multi-planar MR images, and improving PSNR, SSIM, and NMI by 26.2%, 93.4%, and 25.3% respectively compared to bicubic interpolation</li><li>• Wrote academic paper on proposed reconstruction method</li></ul>	
<b>Research Assistant, Fudan University, Shanghai, China</b>	Mar 2016 – Jul 2017
<ul style="list-style-type: none"><li>• Developed embedded simulation system on Xilinx Zynq-7000 AP SoC with partial reconfiguration techniques; system allows for end-to-end software/hardware co-design project simulation</li><li>• Achieved convenient Wi-Fi connection, flexible development environment, and no network downloading latency</li><li>• Designed embedded server and client PC application that could manage simulation requests from multiple users</li><li>• Designed FPGA circuits using dynamic partial reconfiguration technique to decouple user logic from simulation system's static logic</li><li>• Scheduled user access to on-chip FPGA resources by adopting distributed task queue</li><li>• Wrote paper on research that was published in <i>IEEE 12th International Conference on ASIC, 2017</i></li></ul>	

## ACADEMIC PROJECTS

<b>Computer Theory and System, Sound Localization and Enhancement System Design</b>	Spring 2017
<ul style="list-style-type: none"><li>• Designed data transmission system, which transfers sound data to localization and enhancement devices</li><li>• Negotiated with other teams regarding data interfaces; taught network programming skills to team</li><li>• Developed 13-channel data transmission system with UDP and TCP on 6 devices; designed multithreaded management system</li></ul>	
<b>Electronic System Design, Real-Time Temperature Monitoring System Design</b>	Spring 2017
<ul style="list-style-type: none"><li>• Designed and created double bridge circuit on PCB for temperature signal detection, amplification and filtering</li><li>• Programmed STC single-chip microcomputer to sample and quantize temperature signal; designed interruption mechanism to achieve data communication with host computer and control dynamic display of digital tubes</li><li>• Designed host computer application using Matlab to monitor and visualize temperature record</li></ul>	

## PUBLICATIONS

- Gu, J., Wang, R., Wang, J., Lai, J., Duan, Q. "Remote Embedded Simulation System for SW/HW Co-design Based On Dynamic Partial Reconfiguration", accepted to *IEEE 12th International Conference on ASIC, 2017*.
- Gu, J., Yu, J., Li, Z., Wang, Y., Yang, H., Qiao, Z. "Deep Generative Adversarial Networks for Thin-section Infant MR Image Reconstruction", accepted to *IEEE Access, May, 2019*.

## HONORS

- 4<sup>th</sup> Place in 2019 DAC System Design Contest on Low Power Object Detection 2019
- First Prize Scholarship, Fudan University 2017 – 2018
- Top 5, 2018 HUAWEI & FUTURELAB AI Contest (CV Group) 2018
- Top 11%, 2017 IEEEExtreme Global Programming Competition (out of 3,350 teams worldwide) 2017

- 2nd & 3rd prize, National Mathematical Contest in Modeling

2016, 2017

#### **ADDITIONAL INFORMATION**

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**Computer Skills:** Python, C/C++, CUDA, Matlab, Tensorflow, Verilog, Java, Chisel

**Software:** Microsoft Visual Studio, Linux OS, Xilinx Vivado Design Suite, Matlab, Orcad, SPSS, Hspice, Altium Designer