Applied Physics Letters

Integrated multi-operand electro-optic logic gates for optical computing

Cite as: Appl. Phys. Lett. **115**, 171104 (2019); https://doi.org/10.1063/1.5126517
Submitted: 03 September 2019 . Accepted: 12 October 2019 . Published Online: 22 October 2019

Zhoufeng Ying, Chenghao Feng, Zheng Zhao, Richard Soref, David Pan, and Ray T. Chen

AIP Publishing

Applied Physics Letters ARTICLE scitation.org/journal/apl

Integrated multi-operand electro-optic logic gates for optical computing

Cite as: Appl. Phys. Lett. **115**, 171104 (2019); doi: 10.1063/1.5126517
Submitted: 3 September 2019 · Accepted: 12 October 2019 ·
Published Online: 22 October 2019

Zhoufeng Ying,[1,a)] Chenghao Feng,[1] Zheng Zhao,[2] Richard Soref,[3] David Pan,[2] and Ray T. Chen[1,b)]

AFFILIATIONS

[1]Microelectronics Research Center, The University of Texas at Austin, Austin, Texas 78758, USA
[2]Computer Engineering Research Center, The University of Texas at Austin, Austin, Texas 78705, USA
[3]Department of Engineering, University of Massachusetts Boston, Boston, Massachusetts 02125, USA

[a)]Electronic mail: zfying@utexas.edu
[b)]Electronic mail: chenrt@austin.utexas.edu

ABSTRACT

Integrated optical computing has the potential to enhance the computation abilities in terms of computing speed and power consumption during the post-Moore's law era. As one of the widely investigated approaches, electro-optic logic uses electro-optic switches as the building blocks to achieve complex functions. In this paper, we propose and experimentally demonstrate a multioperand electro-optic logic gate that contains multiple active regions in a single gate to further increase the versatility of gates. Thus, one gate can be controlled by several electrical inputs simultaneously. The ability of multioperand logic gates is thoroughly explored. The detailed comparison shows that the proposed gate can largely improve the circuit performance in terms of the area, latency, power, and insertion loss. We believe the multioperand logic gate has the potential to contribute to a more compact and power-efficient integrated optical computing system.

Billions of transistors have powered the information-technology revolution and driven our modern society for several decades. According to Moore's law, the number of transistors on a certain area doubles every two years or so, which generally leads to the doubling of the performance as well.[1] Unfortunately, it is approaching its end due to the unavoidable physical limit.[2] This slowdown has forced a wide range of research studies on fabrication technology, materials science, computer architecture,[3] and optical computing, which includes quantum computing,[4] optical neuromorphic computing,[5] digital optical computing,[6] etc.

Directed logic is one of the most widely investigated architectures, which utilizes an electronic-photonic hybrid approach to take the full advantage of fast and low-loss propagation of light as well as the maturity and controllability of electronics in an integrated system.[7] It consists of a high-speed optical switch array, and the state of each switch is well controlled by an electrical input logic signal. All the signals will be applied simultaneously, and therefore, the latency will not accumulate.[8] With the development of directed logic, more and more essential components and gates are explored and used, some of which may not meet the strict requirements of directed logic but still have most of the advantages. For example, an all-pass modulator does not automatically generate its inverse at the output. Another example is the one to be proposed and discussed in this paper. Therefore, we adopt a more general terminology of electro-optic logic hereinafter to eliminate the latent confusion.

The progress in the field of electro-optic logic can be divided into at least three parts since it was proposed in 2007.[7] First, thanks to advantages of electro-optic logic as opposed to transistors, researchers have been trying to build up logic modules and circuits using fundamental logic gates such as microrings or microdisk modulators to replace the traditional transistor-based counterparts.[9–14] Many proof-of-concept demonstrations are also carried out.[9,11–13] Second, as various photonic components mature, researchers are able to design a more complex circuit and consider at a higher level. For example, similar to the electrical design automation (EDA), several works regarding electrical-photonics design automation (EPDA) have been published, dedicated to designing and optimizing an electro-optic circuit automatically.[15–18] Third, it is obvious that the performance of the electro-optic logic-based circuits highly relies on the characteristics of the electro-optic logic gate. Any improvement in the modulators could directly benefit the system in terms of dynamic power consumption, propagation latency, and packing density. In addition, the advanced fabrication technology has made the multisegment modulators possible,[19] and a theoretical investigation of the two-arm modulator in

optical computing has shown its potential to dramatically improve the circuit performance.[20]

In this paper, we propose a multioperand logic gate (MOLG), where a single gate can be controlled by several electrical signals with different weights. Functions that can be generated by these types of gates outnumber those from traditional gates. MOLGs also have the advantages of a smaller footprint, lower power consumption, smaller latency, and less loss. A thorough comparison is carried out, and an experimental demonstration is also shown in the end as a proof-of-concept.

Electro-optic logic computing significantly relies on the performance of the modulators, and in many designs, microresonator modulators are adopted due to their compactness and low power consumption. Traditional microresonator-based modulators normally use the carrier dispersion effect in silicon platform to achieve high-speed (over 50 Gbps) modulation with an ultralow power consumption of few femtojoules/bit.[21–23] In addition, multisegment microring modulators for high bandwidth-density optical interconnect have been demonstrated.[19] The introduction of multisegment modulators into optical computing area may open up possibilities for computing circuit design because of the different mechanism of function generation, which will be discussed hereinafter. Figure 1 shows the schematic of resonator-based MOLGs, including a 1×1 gate and a 2×2 gate. Each modulator consists of several active segments controlled by independent signals. We mark the logic gate with n segments as MOLG-n in the following, and Fig. 1 shows the case of an MOLG-4. The dotted line with the position of k represents the operating wavelength. The original spectrum of the resonator lies at λ_1, and it will move rightward with electrical inputs.

Here, we begin with a simple case where all the active regions are identical. With electrical signals applied, we will observe the redshift or blueshift of transmission spectra that are received at the through port or the drop port. The displacement depends on the number of the input logic 1 s. For instance, given that the spectrum of the original state locates at λ_1, the spectrum will move to λ_2 with only one input and move to λ_3 with two inputs and so on. Now when the operating

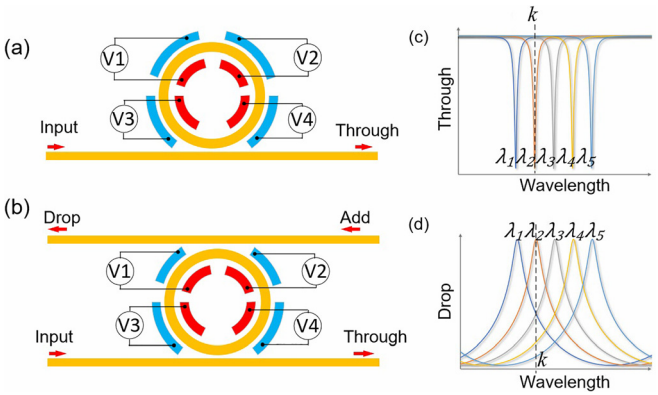

FIG. 1. Schematic of multioperand logic gates. (a) A four-operand 1×1 gate. With different input combinations, the transmission spectrum will shift accordingly as shown in (c). (b) A four-operand 2×2 gate. The spectra at the drop port with different input combinations are shown in (d). The dotted line with the position of k represents the operating wavelength. The original spectrum of the resonator lies at λ_1, and it will move rightward with electrical inputs.

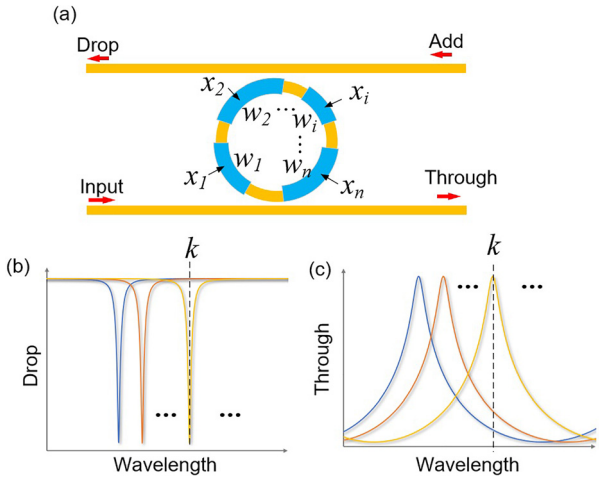

FIG. 2. (a) A general MOLG with weighted inputs with the transmission spectrum at the through port (b) and the drop port (c).

wavelength is set at λ_2, the output will be switched on/off only when only one input is applied. It is noted that different wavelengths lead to different functions.

In this part, we will analyze a general case of the MOLG with weighted segments, as shown in Fig. 2. The logic input applied to the active segment i with the weight of w_i is marked as x_i. The weights can be achieved by the different size of active regions, different driving voltages, or other mechanisms. Assume an electrical signal to each segment will cause a redshift of the transmission spectrum, as shown in Figs. 2(b) and 2(c), and the redshift will accumulate with multiple inputs. When the operating wavelength is set at k, the output will switch its state when the wavelength peak moves exactly to the position of k and only a certain combination of the electrical inputs could match this condition.

Table I shows a general truth table, which contains n columns for n input variables and one column for the output. Each variable could have two logic states, 0 and 1. Therefore, a complete truth table has 2^n rows that illustrate all the possible combinations of the inputs. Each output y_i also has two states, and any combination of y_i along with 2^n input rows represents a logic function. Eventually, n variables could generate 2^{2^n} functions in total.

TABLE I. Truth table.

	Input						Output
No.	x_1	x_2	…	x_i	…	x_n	y
1	x_{11}	x_{12}	…	x_{1i}	…	x_{1n}	y_1
2	x_{21}	x_{22}	…	x_{2i}	…	x_{2n}	y_2
…			…		…		…
j	x_{j1}	x_{j2}	…	x_{ji}	…	x_{jn}	y_j
…			…		…		…
2^n	x_{2^n1}	x_{2^n2}	…	x_{2^ni}	…	x_{2^nn}	y_{2^n}

In row j in the truth table for a MOLG-n at the through port, we have

$$\begin{cases} \sum_{i=1}^{n} w_i x_{ji} = k & \text{for } y_j = 0, \\ \sum_{i=1}^{n} w_i x_{ji} \neq k & \text{for } y_j = 1, \end{cases} \tag{1}$$

where the x_i is the logic input and w_i is a positive weight. k is the position of the operating wavelength. It can also be written as a matrix format like

$$\begin{pmatrix} x_{11} & \cdots & x_{1n} \\ \vdots & \ddots & \vdots \\ x_{2^n} & \cdots & x_{2^n} \end{pmatrix} \begin{pmatrix} w_1 \\ \vdots \\ w_n \end{pmatrix} - k \begin{pmatrix} 1 - y_1 \\ \vdots \\ 1 - y_{2^n} \end{pmatrix} = \begin{pmatrix} t_1 \\ \vdots \\ t_{2^n} \end{pmatrix}, \tag{2}$$

where

$$\begin{cases} t_i = 0 & \text{when } y_j = 0, \\ t_i \neq 0 & \text{when } y_j = 1. \end{cases} \tag{3}$$

The expression at the drop port can be obtained easily by switching y_i between 0 and 1. This matrix equation can be calculated by Matlab to find out all the possible functions. The results are shown in Fig. 3. Taking two-variable case as an example, we could have 10 functions at the through port or the drop port and 16 functions in total when combining two ports after removing the duplicate functions. If compared with the number of 2^{2^n}, we know that the MOLG-1 and MOLG-2 could realize all the functions with one and two variables, respectively. The values for more operands are also calculated, which, however, are not able to catch up with the number of 2^{2^n} since the latter increases extremely fast. Given that field-programmable gate-arrays (FPGAs) mainly consist of lookup tables with sizes in the range of 4–6 inputs,[24] we envision that small-size MOLGs (MOLG-2–MOLG-6) are going to be the main contributors of a complex optical computing system.

Reconfiguration in computing means changing the operating function of a circuit on a chip by simply switching the states of certain components. Reconfiguration in silicon photonics always uses integrated heaters, which makes optical computing circuits more versatile. Figure 4

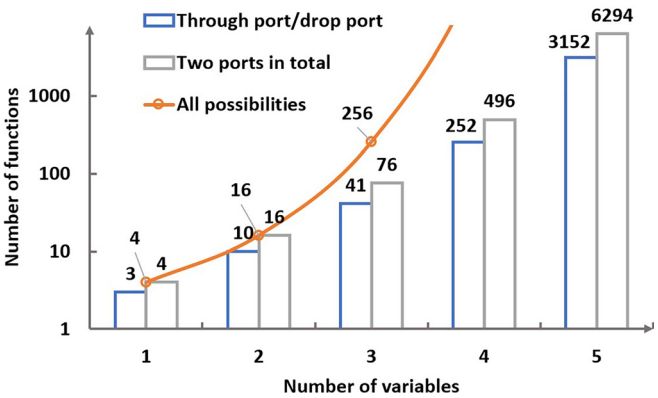

FIG. 3. The number of functions vs the number of variables.

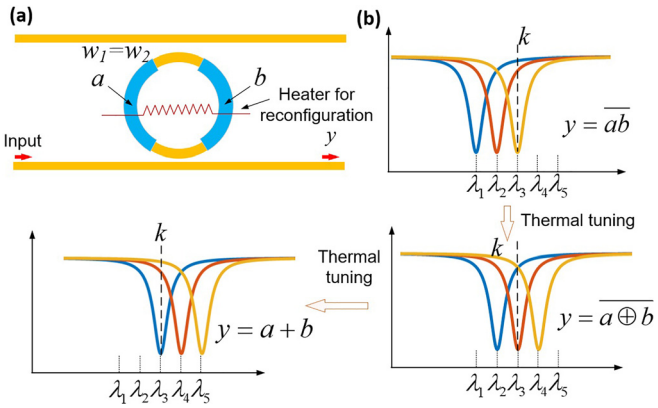

FIG. 4. An example of reconfiguration of an MOLG. At a fixed operating wavelength, a heater could move the spectrum and reconfigure the MOLG to generate different functions.

shows an example of a MOLG equipped with a heater to realize the reconfiguration. It is a MOLG-2 with equal weights, and the electrical input signals are a and b. At input states of (0, 0), (1, 0)/(0, 1), and (1, 1), the transmission spectrum will locate at λ_1, λ_2, and λ_3, respectively. A heater is added on top of the gate. In most instances, the heater will be fabricated on a different layer above the waveguide/device layers so that no influence on the optical performance will be expected. The operating wavelength k is chosen at λ_3. Originally, the function that the MOLG-2 generates is $y = \overline{ab}$. Thermal tuning causes the spectra to redshift, and finally, the function turns out to be $y = \overline{a \oplus b}$ and $y = a + b$, respectively. For a single MOLG, reconfiguration is also achievable by changing the operating wavelength, as shown in the experiment below. However, in a complex system with multiple gates cascaded, using a heater allows for the individual tuning of each gate, which brings more convenience.

MOLGs that squeeze multiple inputs into a single microresonator are capable of generating various logic functions efficiently. In order to quantify the enhancement in terms of the area, dynamic power consumption, latency, and propagation loss, we compare the parameters of several benchmark circuits designed using MOLG-1, MOLG-2, and MOLG-4. The MOLG-1 can be regarded as the conventional logic gate with only one active segment per gate. For simplicity, we assume all the components are in silicon photonics platform, the size of the MOLG-1 is 10 μm × 10 μm, and the areas of MOLG-2 and MOLG-4 are twice and four times larger as that of MOLG-1. The power consumption per active region with the unit length or area is constant, marked as 10 fJ/bit. The insertion loss for any kind of gates is 1 dB no matter at the through port or at the drop port. Each combiner will cause 3 dB insertion loss. All the other loss is ignored. For example, an AND4 circuit consists of 4 MOLGs-1 in a row or 2 MOLGs-2 or 1 MOLG-4. Therefore, the entire insertion loss will be 4 dB, 2 dB, and 1 dB, respectively, due to the insertion loss from each MOLG. Only the propagation delay is considered here, which is proportional to the propagation length. The delay for light to travel through a 10 μm waveguide is around 0.15 ps. The passive splitters or combiners used to connect gates have the width of 10 μm since the radius of the lossless curve for a silicon waveguide is around 5 μm. Note that the

calculation is an estimation and some bends and waveguides that will not affect much the results are neglected.

We select four popular functions as benchmarks, AND4, OR4, XOR4, and XOR-AND, which correspond to the functions of $y = a \cdot b \cdot c \cdot d$, $y = a + b + c + d$, $y = a \oplus b \oplus c \oplus d$, $y = (a \oplus b) \cdot (c \oplus d)$, respectively. From the results shown in Fig. 5, we can see that the MOLG-2 and MOLG-4 provide a much smaller footprint, smaller propagation latency, less dynamic power consumption, and less insertion loss. One of the reasons is that MOLGs could manipulate the weights to achieve a complicated function, while the traditional logic gates have to use sophisticated passive circuits to connect each variable/gate, which brings in lots of complexity and redundancy. Note again that the number of functions that MOLGs can generate is calculated in Fig. 3, and some of the functions are not achievable. For instance, the benchmark of XOR4 in Fig. 5 cannot be built by MOLG-4. Note that the delay caused by resonators is not discussed here, which will be determined by the resonator characteristics as well as the output port. If we take this into consideration, the advantage of MOLGs-4 over MOLGs-1 or MOLGs-2 on latency will be more obvious since it needs fewer gates.

Figure 6 shows the different circuit designs of the function of XOR-AND. A similar reconfigurable design has already been proposed in reference,[25] which uses 4 logic gates (12 resonators). Here, we draw three types of optical computing circuits using MOLGs-1, MOLGs-2, and MOLGs-4, respectively. The first design uses conventional gates and is generated automatically by the binary decision diagram (BDD) algorithm.[18] Redundancy can also be observed due to the special characteristics of the electro-optic logic. The second design utilizes equally weighted MOLG-2, and two cascaded gates will be enough for this target function so that the simpler connection could contribute to a better performance. The last one adopts the MOLG-4 with the weight ratio of 2:2:1:1, and one such kind of gate is all that we need to build the entire circuit, leading to an ultracompact design. The required number of MOLGs-4 is only 16.6% of the required number of MOLGs-1. Further, MOLGs can also be added to the gate library of an AIG-based algorithm for more advanced automated logic synthesis.[17]

Figure 7(a) shows the micrograph of a fabricated MOLG-4 on a silicon-on-insulator (SOI) platform with a 220-nm-thick top silicon

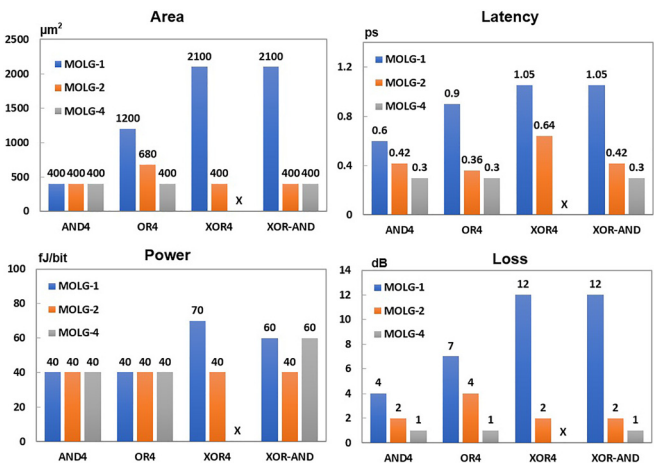

FIG. 5. Comparison in terms of area, latency, power, and loss.

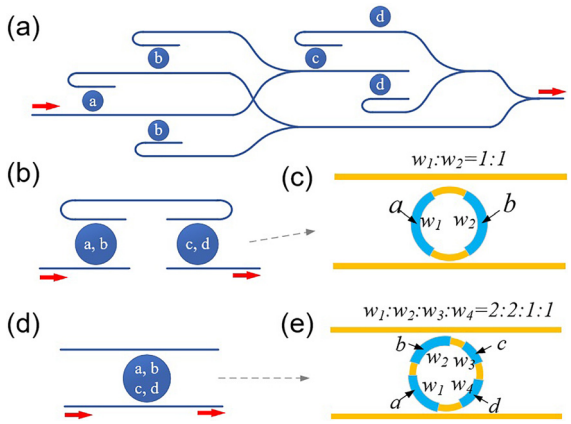

FIG. 6. Circuits design based on (a) MOLGs-1, (b) and (c) MOLGs-2, and (d) and (e) MOLGs-4.

layer. The waveguide is 450 nm in width, and a microring with the radius of 10 μm is adopted here as an example. The quality factor of the microring is 2×10^4. A 1.5 μm-thick isolation layer of SiO_2 is deposited on top of the silicon waveguide. Four identical gold microheaters are fabricated along the microring. As a proof-of-concept, we applied synchronized nonreturn-to-zero (NRZ) electrical signals (a, b) into two of these microheaters. An amplified spontaneous emission (ASE) source and an optical spectrum analyzer (OSA) were first used to measure the transmission spectra at different input combinations (0, 0), (0, 1)/(1, 0), and (1, 1), as shown in Fig. 7(b). Then, we switched to a tunable laser source and finetuned the wavelength to λ_1, λ_2, and λ_3 in sequence. The light was coupled into and out of the chip through grating couplers and finally was received by a photodetector that was connected to an oscilloscope. Figure 7(c) presents the reconfiguration

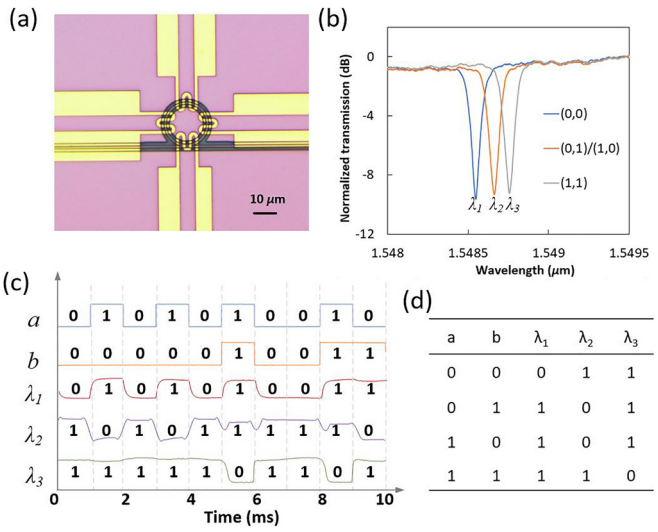

FIG. 7. (a) Micrograph of the fabricated device. (b) The spectra of the MOLG with different input combinations. (c) The testing results at different operating wavelengths. (d) The truth table.

results at three wavelengths with the operating frequency of 1 kbps. The functions realized here are consistent with the truth table in Fig. 7(d) as well as the one in Fig. 4. Note that the output levels for (0, 0) and (1, 1) are slightly different at λ_2, which is because the operating wavelength deviates from expectation. Specifically, it is slightly larger than λ_2 in this case. The reconfiguration is achieved by tuning the operating wavelength, and it should be noted that reconfiguration is also achievable by applying an electrical signal to another microheater.

In conclusion, we have proposed and experimentally demonstrated a multioperand logic gate that could be controlled by multiple logic inputs simultaneously. A thorough calculation is carried out to explore its potential in function generation, and the results show that MOLGs outperform a conventional single-operand logic gate in terms of area, power consumption, latency, and insertion loss. This paves the way for future ultracompact and power-efficient integrated optical computing systems.

The authors acknowledge support from the Multidisciplinary University Research Initiative (MURI) program through the Air Force Office of Scientific Research (AFOSR) (Grant No. FA 9550-17-1-0071), monitored by Dr. Gernot S. Pomrenke.

REFERENCES

[1]D. E. Nikonov and I. A. Young, "Overview of beyond-CMOS devices and a uniform methodology for their benchmarking," Proc. IEEE **101**, 2498–2533 (2013).
[2]M. M. Waldrop, "More than Moore," Nature **530**, 144–148 (2016).
[3]N. H. Weste and D. Harris, *CMOS VLSI Design: A Circuits and Systems Perspective* (Pearson Education India, 2015).
[4]S. Debnath, N. M. Linke, C. Figgatt, K. A. Landsman, K. Wright, and C. Monroe, "Demonstration of a small programmable quantum computer with atomic qubits," Nature **536**, 63 (2016).
[5]Y. Shen, N. C. Harris, S. Skirlo, M. Prabhu, T. Baehr-Jones, M. Hochberg, X. Sun, S. Zhao, H. Larochelle, D. Englund *et al.*, "Deep learning with coherent nanophotonic circuits," Nat. Photonics **11**, 441 (2017).
[6]P. Singh, D. K. Tripathi, S. Jaiswal, and H. Dixit, "All-optical logic gates: Designs, classification, and comparison," Adv. Opt. Technol. **2014**, 1–13.
[7]J. Hardy and J. Shamir, "Optics inspired logic architecture," Opt. Express **15**, 150–165 (2007).
[8]Z. Ying, S. Dhar, Z. Zhao, C. Feng, R. Mital, C.-J. Chung, D. Z. Pan, R. A. Soref, and R. T. Chen, "Electro-optic ripple-carry adder in integrated silicon photonics for optical computing," IEEE J. Sel. Top. Quantum Electron. **24**, 1–10 (2018).
[9]Z. Liu, X. Wu, H. Xiao, X. Han, W. Chen, M. Liao, T. Zhao, H. Jia, J. Yang, and Y. Tian, "On-chip optical parity checker using silicon photonic integrated circuits," Nanophotonics **7**, 1939–1948 (2018).
[10]L. Yang, R. Ji, L. Zhang, J. Ding, and Q. Xu, "On-chip CMOS-compatible optical signal processor," Opt. Express **20**, 13560–13565 (2012).
[11]Z. Ying, Z. Wang, Z. Zhao, S. Dhar, D. Z. Pan, R. Soref, and R. T. Chen, "Silicon microdisk-based full adders for optical computing," Opt. Lett. **43**, 983–986 (2018).
[12]C. Qiu, X. Ye, R. Soref, L. Yang, and Q. Xu, "Demonstration of reconfigurable electro-optical logic with silicon photonic integrated circuits," Opt. Lett. **37**, 3942–3944 (2012).
[13]L. Zhang, R. Ji, L. Jia, L. Yang, P. Zhou, Y. Tian, P. Chen, Y. Lu, Z. Jiang, Y. Liu *et al.*, "Demonstration of directed XOR/XNOR logic gates using two cascaded microring resonators," Opt. Lett. **35**, 1620–1622 (2010).
[14]Y. Tian, L. Zhang, R. Ji, L. Yang, P. Zhou, H. Chen, J. Ding, W. Zhu, Y. Lu, L. Jia *et al.*, "Proof of concept of directed OR/NOR and AND/NAND logic circuit consisting of two parallel microring resonators," Opt. Lett. **36**, 1650–1652 (2011).
[15]R. Wille, O. Keszocze, C. Hopfmuller, and R. Drechsler, "Reverse BDD-based synthesis for splitter-free optical circuits," in *20th Asia and South Pacific Design Automation Conference* (IEEE, 2015), pp. 172–177.
[16]C. Condrat, P. Kalla, and S. Blair, "Logic synthesis for integrated optics," in *Proceedings of the 21st Edition of the Great Lakes Symposium on Great Lakes Symposium on VLSI* (ACM, 2011), pp. 13–18.
[17]Z. Ying, Z. Zhao, C. Feng, R. Mital, S. Dhar, D. Z. Pan, R. Soref, and R. T. Chen, "Automated logic synthesis for electro-optic logic-based integrated optical computing," Opt. Express **26**, 28002–28012 (2018).
[18]Z. Zhao, Z. Wang, Z. Ying, S. Dhar, R. T. Chen, and D. Z. Pan, "Optical computing on silicon-on-insulator-based photonic integrated circuits," in *2017 IEEE 12th International Conference on ASIC (ASICON)* (IEEE, 2017), pp. 472–475.
[19]A. Roshan-Zamir, B. Wang, S. Telaprolu, K. Yu, C. Li, M. A. Seyedi, M. Fiorentino, R. Beausoleil, and S. Palermo, "A two-segment optical DAC 40 Gb/s PAM4 silicon microring resonator modulator transmitter in 65 nm CMOS," in *2017 IEEE Optical Interconnects Conference (OI)* (IEEE, 2017), pp. 5–6.
[20]D. Gostimirovic and N. Y. Winnie, "Ultracompact CMOS-compatible optical logic using carrier depletion in microdisk resonators," Sci. Rep. **7**, 12603 (2017).
[21]E. Timurdogan, C. M. Sorace-Agaskar, J. Sun, E. S. Hosseini, A. Biberman, and M. R. Watts, "An ultralow power athermal silicon modulator," Nat. Commun. **5**, 4008 (2014).
[22]Z. Ying, Z. Wang, Z. Zhao, S. Dhar, D. Z. Pan, R. Soref, and R. T. Chen, "Comparison of microrings and microdisks for high-speed optical modulation in silicon photonics," Appl. Phys. Lett. **112**, 111108 (2018).
[23]M. Pantouvaki, P. Verheyen, J. De Coster, G. Lepage, P. Absil, and J. Van Campenhout, "56 Gb/s ring modulator on a 300 mm silicon photonics platform," in *2015 European Conference on Optical Communication (ECOC)* (IEEE, 2015), pp. 1–3.
[24]E. Ahmed and J. Rose, "The effect of LUT and cluster size on deep-submicron FPGA performance and density," IEEE Trans. Very Large Scale Integr. Syst. **12**, 288–298 (2004).
[25]Q. Xu and R. Soref, "Reconfigurable optical directed-logic circuits using microresonator-based optical switches," Opt. Express **19**, 5244–5259 (2011).